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S5U13T04P00C100
Evaluation Board User Manual

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SEIKO EPSON CORPORATION Rev. 1.0

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1 Introduction

This manual describes the setup and operation of the S5U13T04P00C100 reference board.

This reference board is designed as an evaluation platform for the S1D13T04 EPD Timing Controller. The S5U13T04P00C100 reference board has a host interface connector, EPD panel connector, and a 2.0 inch EPD panel.

This user manual is updated as appropriate. Please check the Seiko Epson Website at http://www.epson.jp/device/semicon_e/product/lcd_controllers/index.htm for the latest revision of this document before beginning any development.

We appreciate your comments on our documentation. Please contact us via email at documentation@erd.epson.com.

2 Features

The S5U13T04P00C100 reference board includes the following features:

- Supports SPI host interface
- Epson’s S1D13T04 EPD Timing Controller.
- Power connector
- Panel Interface connector.
- 2.0 inch EPD panel.

3 Setup and Configuration

The main functional blocks of the evaluation board are shown below.

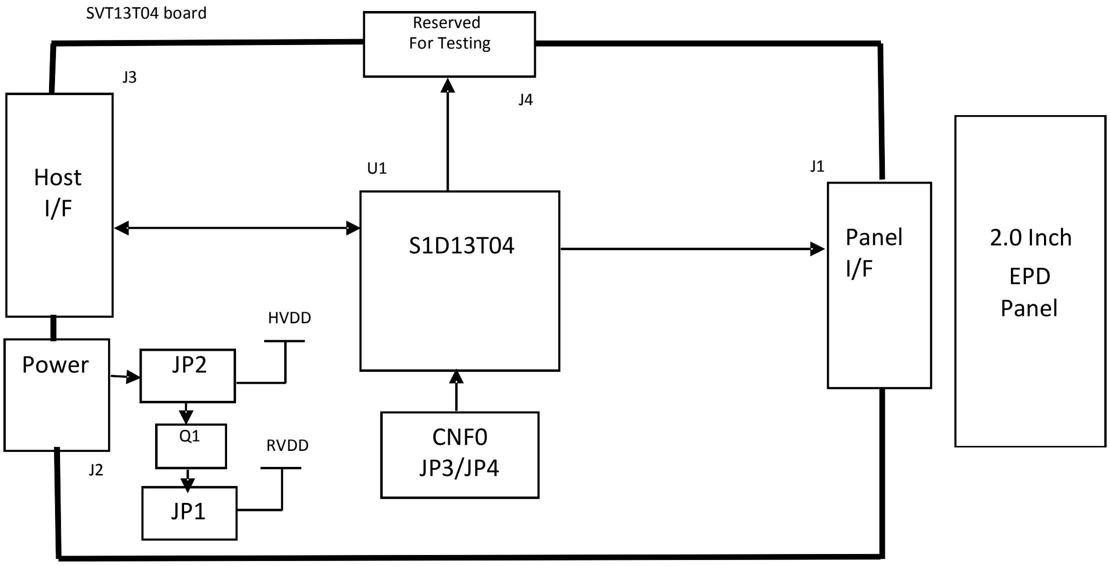


Figure 3-1 S5U13T04P00C100 Reference Board Block Diagram

CNF0 is configured with jumpers JP3 and JP4 as shown in the following table.

Table 3-1 CNF0 Configuration Selection

CNF0	JP3	JP4	Comments
0	Open	Short	H_RDY signal is all ways driven (Default)
1	Short	Open	H_RDY signal is open drain signal

4 Connectors

The S5U13T04P00C100 reference board has four connectors for Host Interface, Panel Interface, Power and Reserved for Production Test (J1, J2, J3 and J4). The location of these connectors is shown in the following figure.

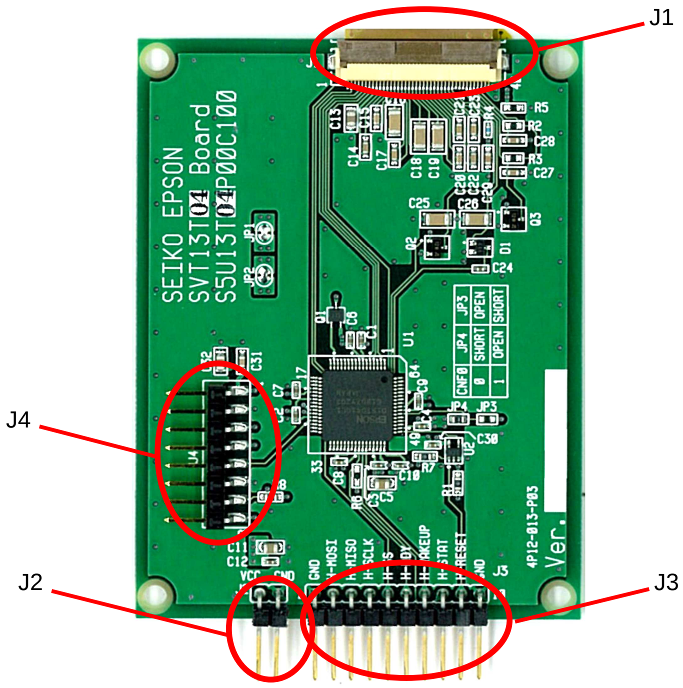


Figure 4-1 S5U13T04P00C100 Reference Board Top View / Connector Locations



Figure 4-2 S5U13T04P00C100 Reference Board Bottom View

4.1 J1 Panel Interface Connector

The panel interface pins of the S1D13T04 are connected through J2.

Table 4-1 J1 Panel Interface Connector

Connector	: J1				
Manufacture	: HIROSE FH12S-40S-0.5SH 40pin				
Pin No.	**Signal Name**	**Description**	**Pin No.**	**Signal Name**	**Description**
1	CSB	EPD Chip Select	21	C15P	Charge Pump Capacitor
2	BUSY	EPD BUSY	22	C14M	Charge Pump Capacitor
3	ID	Set ID to 0	23	C14P	
4	SCLK	Serial Clock	24	C13M	Charge Pump Capacitor
5	SI	Serial data output	25	C13P	
6	SO	Serial data input	26	C12M	Charge Pump Capacitor
7	RESETB	EPD Reset	27	C12P	
8	ADC_IN	N.C.	28	C11M	Charge Pump Capacitor
9	VCL	EPD VCL Capacitor	29	C11P	
10	C42P	Charge Pump Capacitor	30	VCOM_DRIVER	VCOM from Driver IC
11	C42M		31	VCC	+3.3V for analog
12	C41P	Charge Pump Capacitor	32	VDD	+3.3V for digital
13	C41M		33	GND	Ground
14	C31P	Charge Pump Capacitor	34	VGH	EPD VGH
15	C31M		35	VGL	EPD VGL
16	C21P	Charge Pump Capacitor	36	VDH	EPD VDH
17	C21M		37	VDL	EPD VDL
18	C16P	Charge Pump Capacitor	38	BORDER	EPD BORDER
19	C16M		39	VST	EPD VST
20	C15M	Charge Pump Capacitor	40	VCOM_PANEL	EPD VCOM

4.2 J2 Power Connector

Power for the S5U13T04P00C100 Evaluation Board is supplied through J2.

Table 4-2 J2 Panel Interface Connector

Pin No.	Signal Name	Description
1	VCC	Power supply +3.0V
2	GND	Ground

4.3 J3 Host Interface Connector

The host interface pins of the S1D13T04 are connected through J3.

Table 4-3 J3 Host Interface Connector

Pin No.	Signal Name	Direction	Description
1	GND	Power	Ground
2	H-MOSI	Input	SPI interface master to slave data
3	H-MISO	Output	SPI interface slave to master data
4	H-SCLK	Input	SPI interface serialize clock
5	H-SS	Input	SPI interface slave select signal
6	H-RDY	Output	0 = S1D13T04 is busy 1 = S1D13T04 is ready
7	H-WAKEUP	Input	0 = Puts the S1D13T04 in sleep mode 1 = Puts the S1D13T04 in run mode
8	H-STAT	Output	0 = S1D13T04 is in sleep mode 1 = S1D13T04 is in run mode
9	H-RESET	Input	0 = Reset is active 1 = Reset is inactive
10	GND	Power	Ground

4.4 J4 Production Test Connector

J4 is reserved for Production Testing and should not be used.

5 Parts List

Table 5-1 S5U13T04P00C100 Bill of Materials

Item	Quantity	Reference	Part	Manufacture	Description
1	1	D1	BAT54SW	NXP	
2	1	J1	FH12S-40S-0.5SH(55)	HIROSE	
3	2	Q3,Q2	2N7002	NXP	
4	1	Q1	ZXMP6A13FTA	DIODES Inc.	
5	1	U2	SN74LVC1G08IDCKR	Texas Instruments	
6	1	U1	S1D13T04	EPSON	P-TQFP064-1010-0.50
7	2	C11,C32	GRM21BB31A106KE18L	MURATA	2012 10uF ±10% DC10V
8	11	C1,C2,C3,C4,C6, C7,C8,C9,C10, C12,C30	GRM155B11A104K	MURATA	1005 0.1uF ±10% DC16V
9	1	C5	GRM21BB31E475KAL75L	MURATA	2012 4.7uF ±10% DC25V
10	1	C31	GRM188B11E104KA01	MURATA	1608 0.1uF ±10% DC25V
11	1	C13	GRM21BF61A225KA01	MURATA	2012 2.2uF ±10% DC10V X5R
12	7	C14,C15,C17, C20,C21,C22, C23	GRM188F61C225KE15	MURATA	1608 2.2uF ±10% DC16V X5R
13	2	C27,C28	GRM188F61C225KA12	MURATA	1608 2.2uF ±10% DC25V X5R
14	5	C16,C18,C19, C25,C26	GRM319F61E225KA12	MURATA	3216 2.2uF ±10% DC25V X5R
15	1	C24	GRM155R11C104KA88D	MURATA	1005 0.1uF ±10% DC16V
16	1	C29	GRM188R71A105KA61	MURATA	1608 1uF ±10% DC16V
17	3	R1,R7,R8	RK73B1JTTP1002F	KOA	1608 10.0K ±5% 0.063W
18	1	R4	RK73B1ETTP202J	KOA	1005 2.0K ±5% 0.063W
19	1	R5	RK73B1JTTD333J	KOA	Nomount (1608 33K ±5% 0.1W)
20	1	JP4	RK73Z1JTTD	KOA	1608 0 — 1A
21	1	J2	6-102974-0	TE	2/10 -pin
22	1	J3	6-102974-0	TE	10-pin
23	1	J4	961108-5500-AR-PR	3M	10-pin
24	1		—	—	2.0inch EPD panel
25	3	JP3,R2,R3	RK73Z1JTTD	KOA	Nomount (1608 0 — 1A)
26	1	R6	RK73B1JTTD103J	KOA	Nomount (1608 10K — 1A)

6 Schematic Diagram

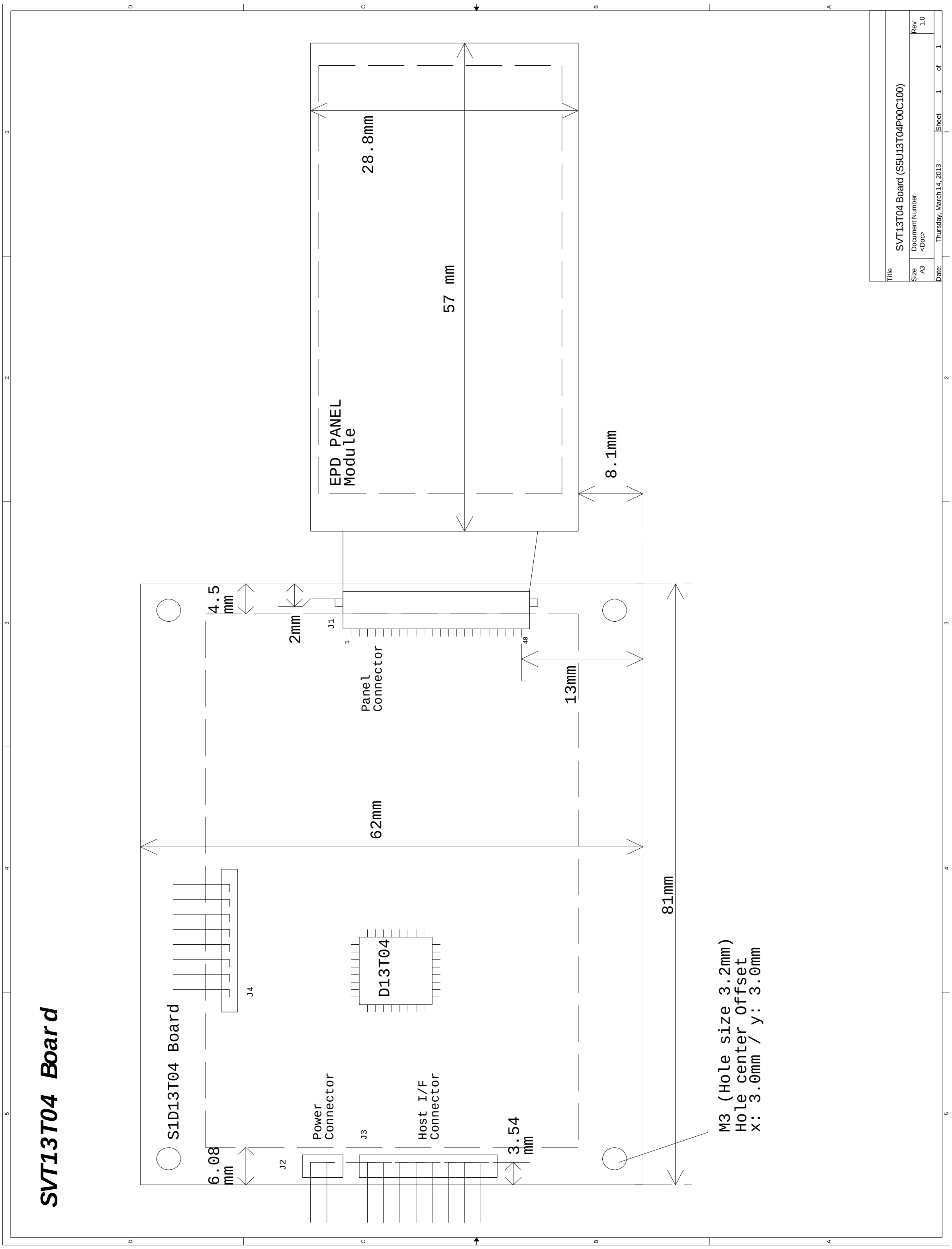


Figure 6-1 S5U13T04P00C100 Schematic Diagram (1 of 2)

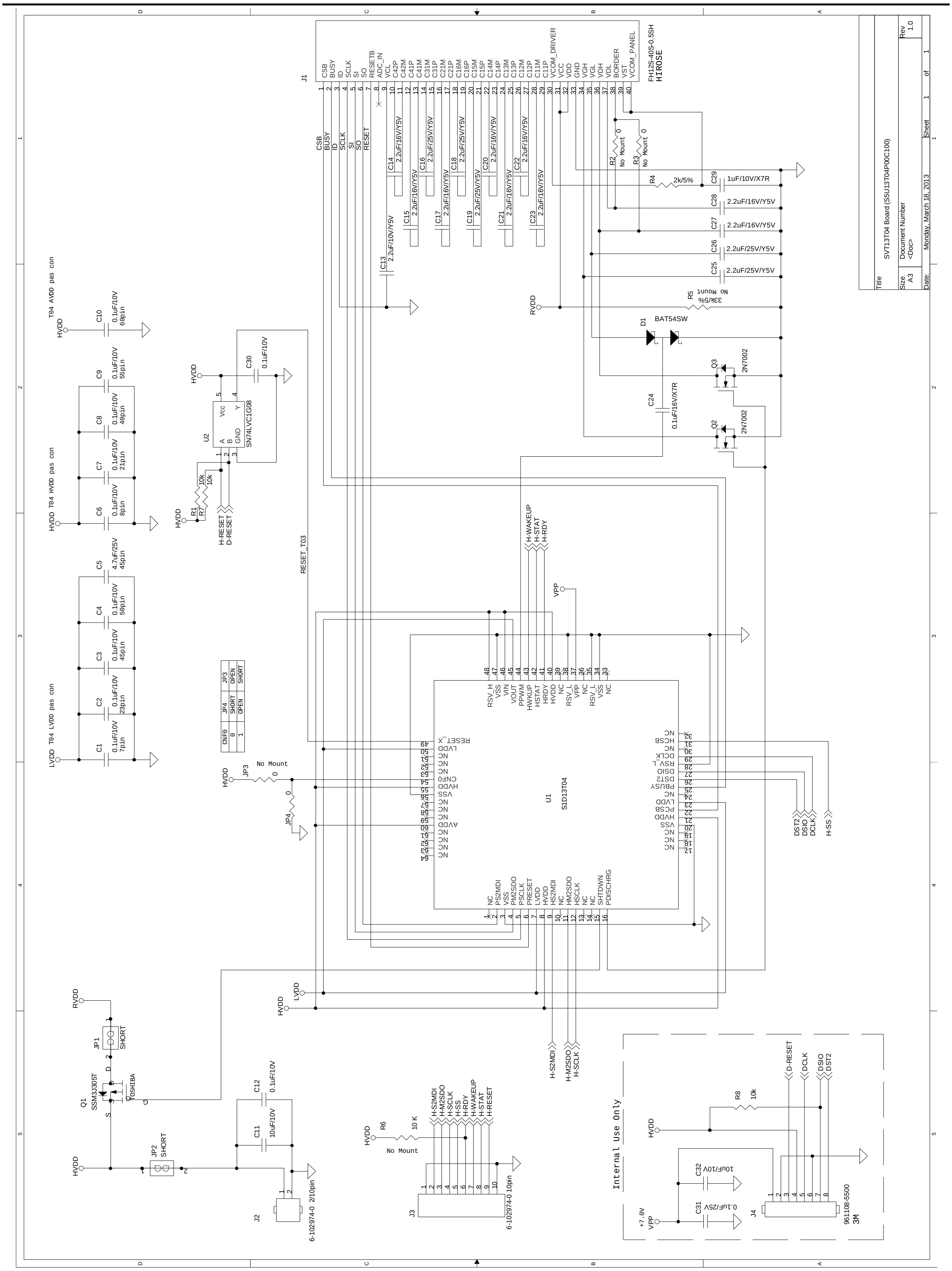


Figure 6-2 S5U13T04P00C100 Schematic Diagram (2 of 2)

7 References

Epson Research and Development, Inc., S1D13T04 Hardware Functional Specification, document number XA3A-A-001-xx.

8 Change Record

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